M1706

16-Bit Digital I/O M-Module

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This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.

Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.

Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.

2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until, performance is checked by qualified personnel.

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Chapter 1
Getting Started

What's in this Manual?

This manual contains a module description, configuration and wiring information, register maps, and specifications for the M-Module.

- Racal M1706 16-Bit Digital I/O Module (P/N 407876)

The Racal M1706 is intended to be installed on an M-Module Carrier. When it is necessary to reference a particular carrier, the C&H Technologies Model VX405C C-Size VXIbus M-Module Carrier will be used. Refer to the User Manual for the M-Module Carrier used for installation instructions.

Module Description

The Racal M1706 is a digital input/output M-Module containing 16 data/actuator lines. These data lines offer TTL compatible inputs and open-drain outputs up to 30 volts. Each I/O line also provides active pull-up and pull-down for actuating external devices such as:

- Relays and switches
- High frequency coax relays or microwave switches
- Programmable attenuators
- Optical Isolators

Racal M1706 Features

- Sixteen Digital Inputs or Outputs. Data that is written (output) may also be read back. Bits may be addressed as two 8-bit ports (Port 0 and Port 1), one 16-bit port (Port 0), or individual bits can be accessed.

- Support of M-Module Specification Type C Interrupts for pattern matching. An interrupt occurs (if enabled) when the incoming data matches the pattern stored in the Compare Data Register.

- Debounce capability for data lines used as inputs. The debounce circuitry allows incoming data to be debounced for a period of 3 mSec before being latched into the Input Register. You can enable/disable debounce for the Input Register, however, debounce is always active for the input to the pattern match interrupt circuit.

- TTL compatible levels or open-drain outputs. The 16 data lines provide for TTL compatible I/O (open-drain outputs up to 30 Volts, requires external pull-up).

- There are no I/O handshaking lines/modes.

Output Circuitry

Figure 1-1 shows a simplified schematic of one bit's output circuitry and two example applications. For the driver commands, sourcing a "1" means that the output is driven high (2.9 Vdc or greater, sourcing up to 20 mA); sourcing a "0" means the output is driven low (0.4 Vdc or less, sinking up to 200mA).

Caution **Do not exceed the 30Vdc external voltage; doing so may damage the module.**

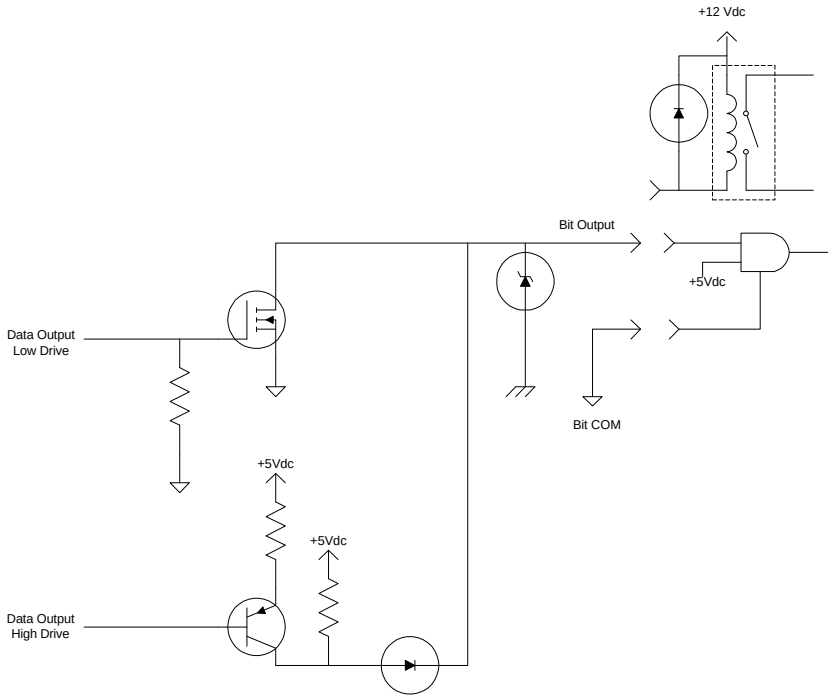


Figure 1-1. Simplified Digital Output Circuit

Input Circuitry

Figure 1-2 shows a simplified schematic of one bit's input circuitry and two example applications. Because the input bit has its own pull-up resistor, the bit can be used to detect switch closures to ground. Using external pull-ups, it can also be used with digital logic "high" levels of up to 30 Vdc. When used as digital inputs, a "HIGH" or "1" means a positive voltage (>1.8 Vdc) is present and "LOW" or "0" means a voltage of <0.8 Vdc is present.

Caution **Do not exceed the 30Vdc external voltage; doing so may damage the module.**

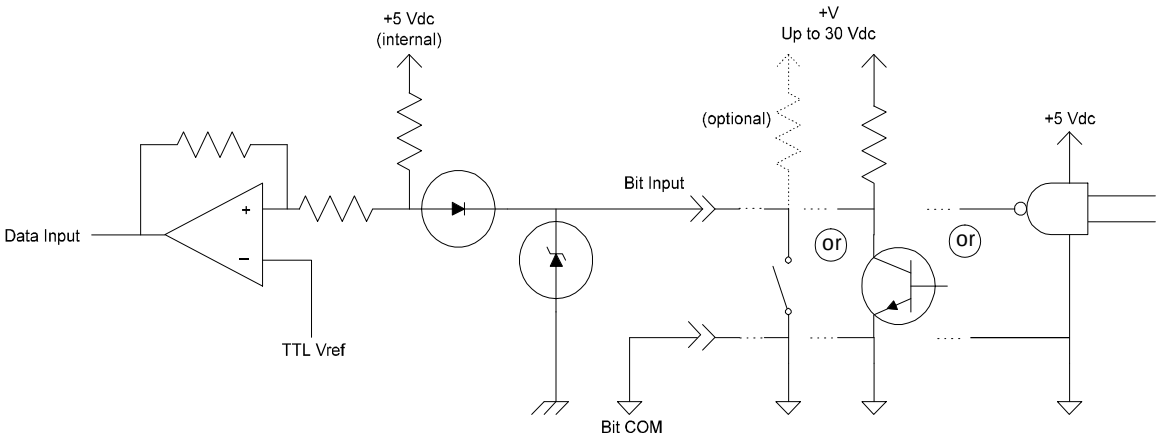


Figure 1-2. Simplified Digital Input Circuit

Wiring and Configuration

This section describes how to connect user wiring to Racal M1706.

Note The procedures in this section assume the M-Module(s) have already been installed into an M-Module Carrier. Since installation is dependent on the carrier used, instructions for installing M-Modules into the carrier are not included here. Refer to your M-Module carrier documentation for installation instructions.

WARNING **SHOCK HAZARD. Only service-trained personnel who are aware of the hazards involved should install, remove, or configure the modules. Before installing or removing any module or carrier, disconnect power from the mainframe and user wiring.**

Caution **MAXIMUM VOLTAGE/CURRENT. Maximum voltage that may be applied (any I/O line to chassis) to the Racal M1706 is 30 VDC.**

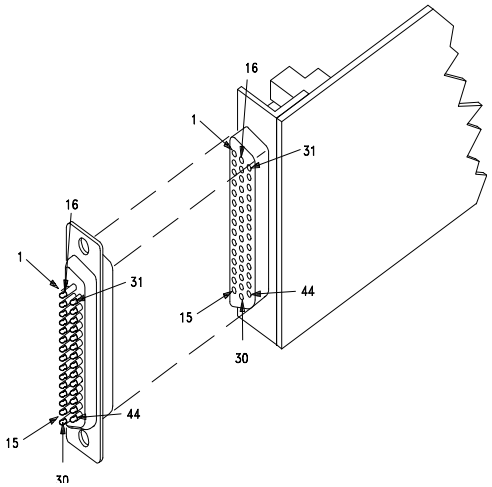
Caution **STATIC ELECTRICITY. Static electricity is a major cause of component failure. To prevent damage to the electrical components on an M-Module or the carrier, observe anti-static techniques whenever installing, removing, or working on a carrier or M-Module.**

Wiring to the Supplied Mating Connector

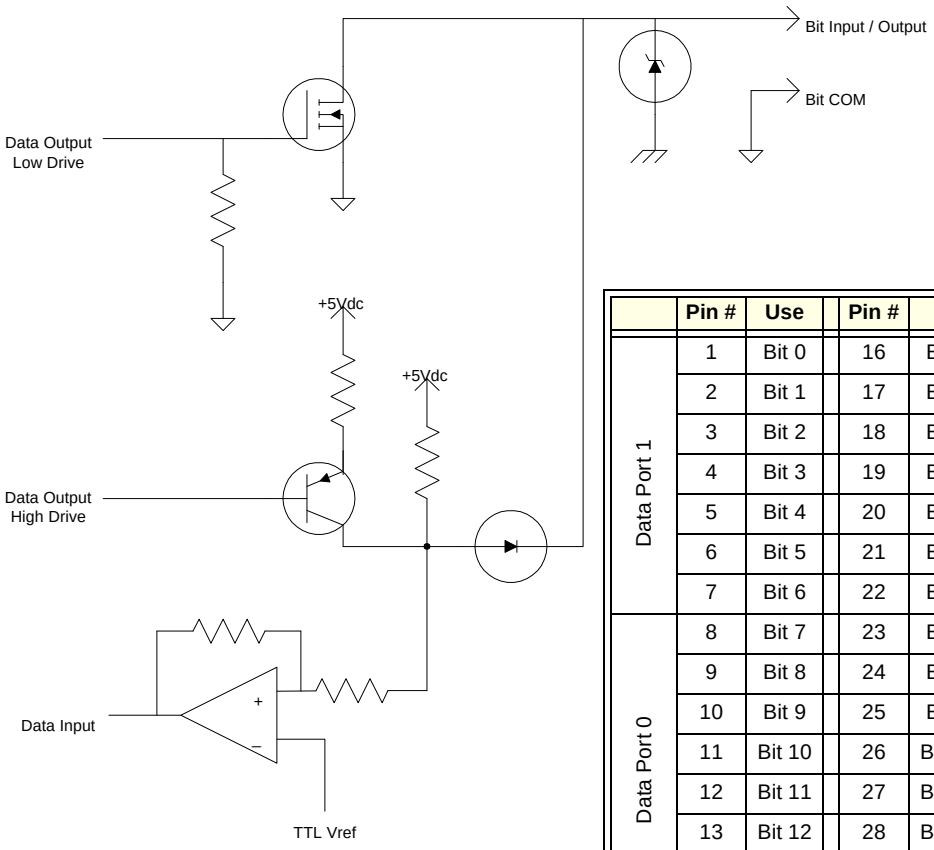
Figure 1-3 shows the 44-pin user connector, its pinout, and a simplified schematic for the input/output circuitry. Figure 1-4 shows how to wire and assemble the supplied connector and hood.

Note Do not use the supplied hood if the Racal M1706 is installed in one of the two internal slots (Positions E or F) of the C&H Technologies Model VX405C M-Module Carrier.

Racal M1706 Digital I/O Wiring Information



CAUTION The maximum voltage is 30 VDC (any I/O line to chassis or common).



	Pin #	Use	Pin #	Use	Pin #	Use
Data Port 1	1	Bit 0	16	Bit 0 COM	31	Chassis
	2	Bit 1	17	Bit 1 COM	32	Chassis
	3	Bit 2	18	Bit 2 COM	33	Chassis
	4	Bit 3	19	Bit 3 COM	34	Chassis
	5	Bit 4	20	Bit 4 COM	35	Chassis
	6	Bit 5	21	Bit 5 COM	36	Chassis
	7	Bit 6	22	Bit 6 COM	37	Chassis
Data Port 0	8	Bit 7	23	Bit 7 COM	38	Chassis
	9	Bit 8	24	Bit 8 COM	39	Chassis
	10	Bit 9	25	Bit 9 COM	40	Chassis
	11	Bit 10	26	Bit 10 COM	41	Chassis
	12	Bit 11	27	Bit 11 COM	42	Chassis
	13	Bit 12	28	Bit 12 COM	43	Bit 15
	14	Bit 13	29	Bit 13 COM	44	Bit 15 COM
	15	Bit 14	30	Bit 14 COM		

Figure 1-3. Racal M1706 User Connector and I/O Schematic

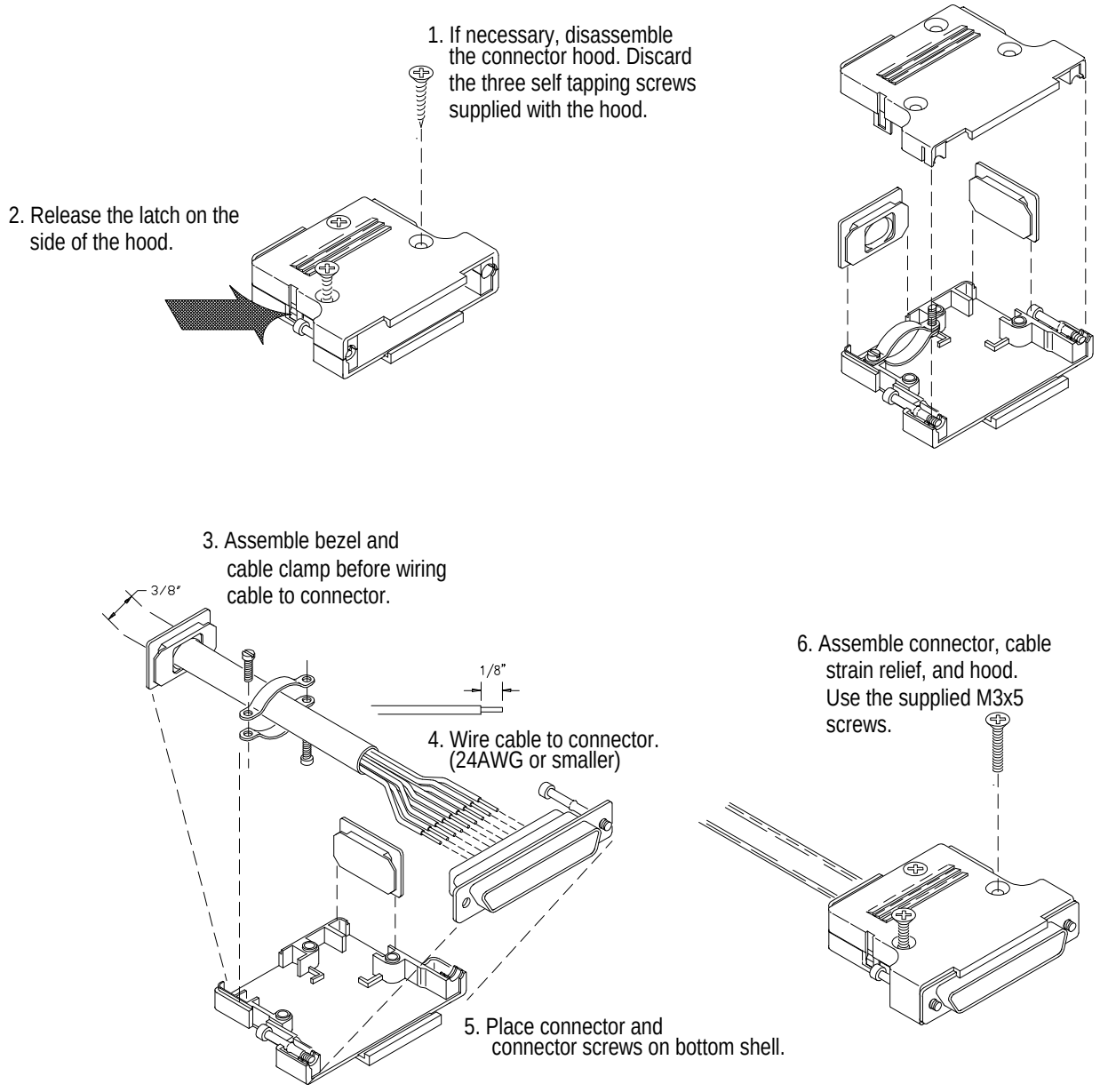


Figure 1-4. Assembling the Connector and Hood

Note Do not use the supplied hood if the Racal M1706 is installed in one of the two internal slots (Positions E or F) of the C&H Technologies Model VX405C M-Module Carrier.

Chapter 2
Register Programming

Introduction

This chapter describes how to program the Racal M1706 Digital I/O M-Module at the register level in an C&H Technologies Model VX405C Carrier installed in a VXIbus mainframe. Register programming is recommended only if you are unable to use the module's higher-level VXI*plug&play* driver. For information on using the VXI*plug&play* driver, refer to the included help files.

Block Diagram Description

In order to register program the Racal M1706, it is important to understand its operation at the block diagram level. Figure 2-1 shows a simplified block diagram of the module.

Module Control

This block contains all of the logic for the module including all registers, interrupt control, and carrier interface.

ID EEPROM

The EEPROM holds sixty-four 16-bit words of M-Module ID data and VXI M-module data. Refer to "ID EEPROM Register" on page 2-16 for EEPROM contents.

Input Circuit

The input comparator maintains correct TTL high and low levels by shifting the input voltages to compensate for the forward voltage drop of the blocking diode. A reference voltage of +1.9Vdc is applied to the inverting input of the comparator. When the input is in the range of 0Vdc to +4.3Vdc the blocking diode is forward biased, and its forward voltage drop is added to the applied voltage. For example, when 0Vdc is applied to the data line, +0.7Vdc is present on the comparator's non-inverting input. Similarly, when the input signal is greater than +1.2Vdc, a voltage greater than +1.9 Vdc is applied to the comparator's non-inverting input causing its output to go high. When the applied voltage is less than +1.2Vdc, a voltage less than +1.9Vdc is applied to the comparator causing its output to be low.

The pull-up resistor on the comparator's non-inverting input allows external ground connections and open circuits to be detected.

High Drive Circuit

The high drive circuit (active when sourcing a high, 2.9 Vdc) consists of a blocking diode and a PNP transistor circuit for each line. The transistor is in a high impedance state when the line is not output-enabled or the line is driving low.

Low Drive Circuit

The low drive circuit (active when sourcing a low, 0.4Vdc) consists of one MOSFET, and a pull-down resistor. The MOSFET is in a high impedance state when the line is not output-enabled or the line is driving high. During a low level output, the MOSFET is turned on creating a low impedance path from the channel input to channel common. The MOSFET can sink up to 200mA.

Ground and Power Supply Conditioning

This block filters the +5Vdc power to produce the VCC power necessary for the logic circuity and isolates the various grounds used by the module. The module does not use ±12Vdc power.

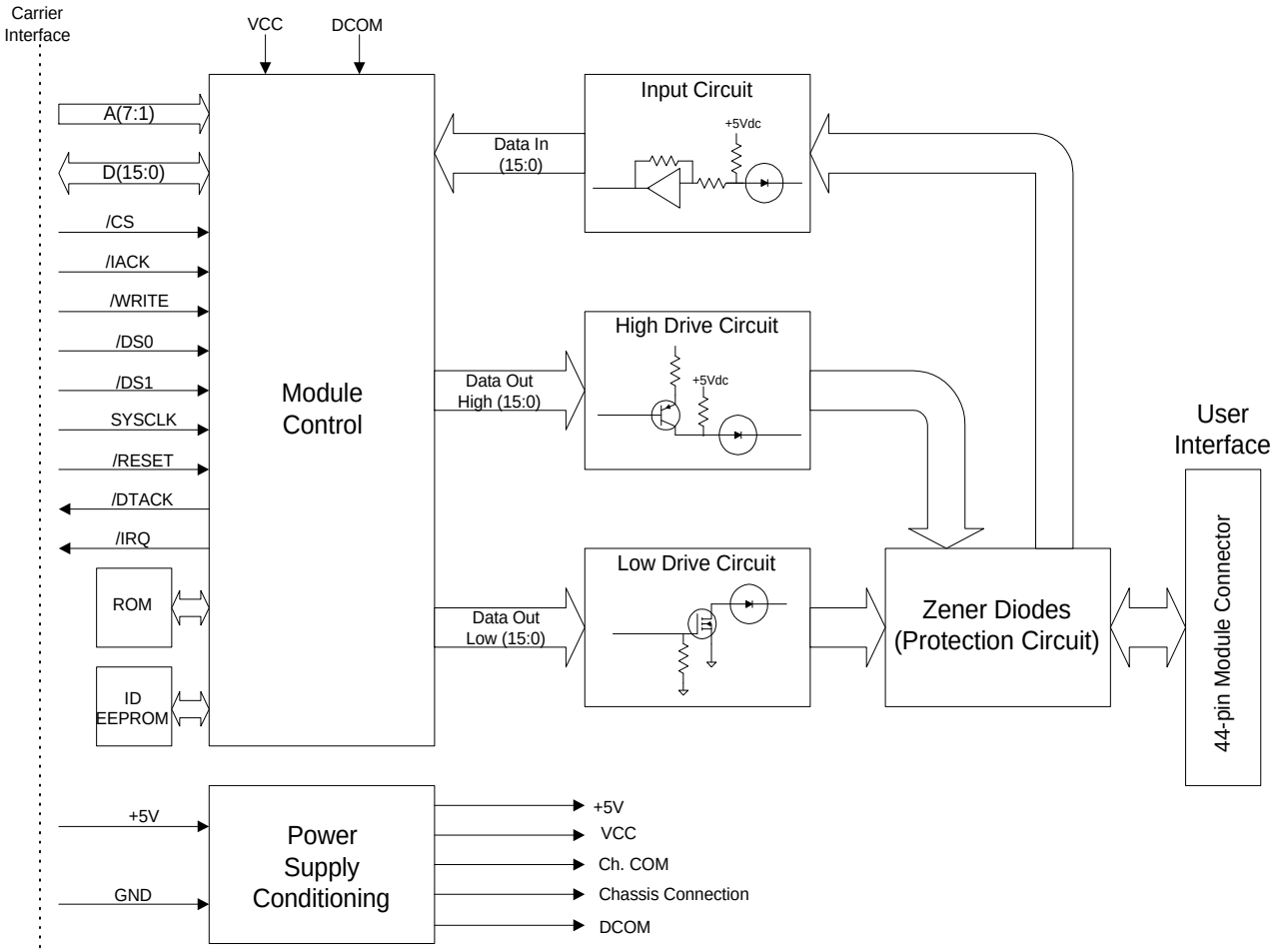


Figure 2-1. Racal M1706 Simplified Block Diagram

Register Addressing in the VXIbus Environment

Logical Address

Each module in a VXIbus (VXI) system, whether VXI or M-Module, must have a unique logical address. The C&H Technologies Model VX405C Carrier provides a logical address for each installed M-Module. Refer to the VX405C Installation Section for details (if you are using a different carrier, refer to that carrier's documentation for register-based addressing information).

A16/A24 Memory Mapping

The VXI Specification allows for only 64 bytes of address space in A16 memory. However, the M-Module Specification defines 256 bytes of address space. To resolve this conflict, the VX405C Carrier provides two memory segments for each installed M-Module. The first is in the VXI A16 memory space and contains the standard VXI registers. The second memory segment is in the VXI A24 memory space and contains all other M-Module registers (these registers are described starting on page 2-9). Figure 2-2 on page 2-4 shows the A16/A24 mapping for a typical M-Module.

Note

The M-Module's ID word (from the ID EEPROM) is mapped into the VXI Manufacturer ID Register at address 00_h and the M-Module's VXI Device Type word is mapped into the VXI Device Type Register at address 02_h

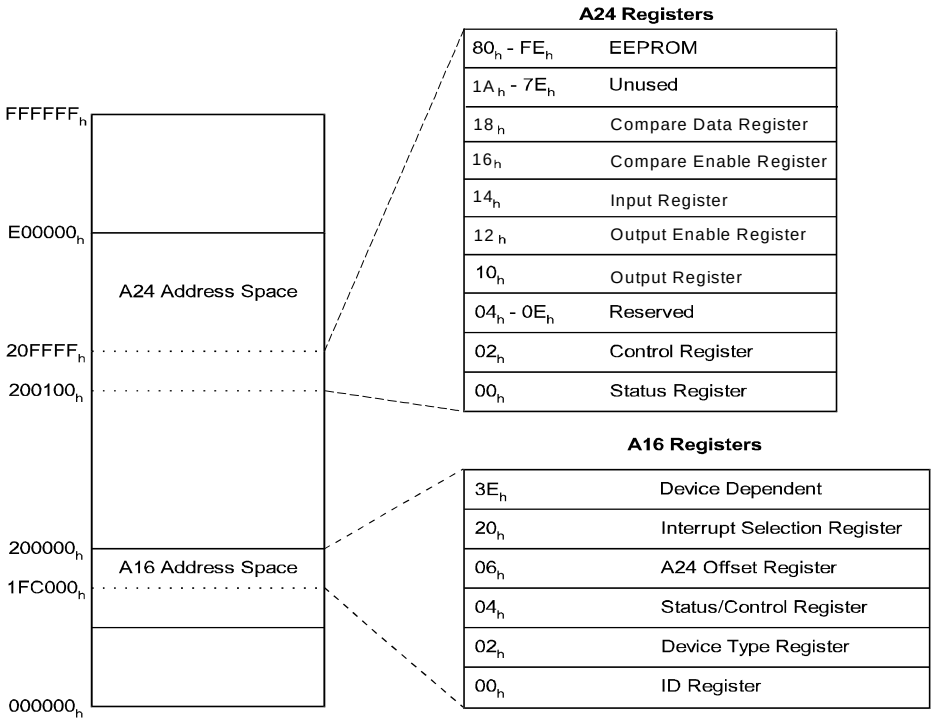


Figure 2-2. A16/A24 Address Mapping

Determining a Module's A16 Base Address

To access a register in A16 memory, you must specify a hexadecimal or decimal register address. This address consists of a base address plus a register offset. The A16 base address depends on whether or not you are using a GPIB Slot 0.

A16 Address Space Inside the Command Module

When <u>using</u> a GPIB Slot 0, the base address is computed as:

$1FC000_h + (LADDR_h \cdot 40_h)$
or (decimal)
$2{,}080{,}768 + (LADDR \cdot 64)$

Where:
$1FC000_h$ (2,080,768) is the A16 starting address
LADDR is the module's logical address
40_h (64) is the number of address bytes allocated per module

For example, if the M-Module has a logical address of 78_h (120) the A16 base address becomes:

$1FC000_h + (78_h \cdot 40_h) = 1FC000_h + 1E00_h = 1FDE00_h$
or (decimal)
$2{,}080{,}768 + (120 \cdot 64) = 2{,}080{,}768 + 7680 = 2{,}088{,}448$

A16 Address Space Outside the Command Module

When a GPIB Slot 0 is <u>not</u> part of your system, the base address is computed as:

$C000_h + (LADDR_h \cdot 40_h)$
or (decimal)
49,152 + (LADDR · 64)

Where:
$C000_h$ (49,152) is the A16 starting address
LADDR is the module's logical address
40_h (64) is the number of address bytes allocated per module

For example, if the M-Module has a logical address of 78_h (120) the A16 base address becomes:

$C000_h + (78_h \cdot 40_h) = C000_h + 1E00_h = DE00_h$
or (decimal)
49,152 + (120 · 64) = 49,152 + 7680 = 56,832

Addressing A16 Registers

As shown in Figure 2-2 on page 2-4, VXI registers for an M-Module are mapped into A16 address space. To access one of these registers, add the A16 base address to the register offset. For example, an M-Module's VXI Status/Control Register has an offset of 04_h. To access this register (assuming the system does not have a GPIB Slot 0 Module), use the register address:

$1FDE00_h + 04_h = 1FDE04_h$
or (decimal)
2,088,488 + 4 = 2,088,452

Addressing A24 Registers

As shown in Figure 2-2 on page 2-4, most of the registers for an M-Module are mapped into A24 address space. To access one of these registers:

1. Obtain the A24 base address by reading the VXI Offset Register (06_h) in A16 memory.

2. Add the A24 base address to the register offset (see Table 2-2).

For example, if the A24 base address is 200100_h, to access the Output Register (10_h):

$200100_h + 10_h = 200110_h$
or (decimal)
2,097,408 + 16 = 2,097,424

Program Example

The following C language program demonstrates how to program at the register level. The program reads the ID, Device Type, Status, and A24 registers then sets bits 00 and 02 to a HI state. This program was written and tested in Microsoft Visual C++ but should compile under any standard ANSI C compiler.

To run this program you must have the NI VISA library, a GPIB interface module installed in your PC, and an GPIB Slot 0 module such as a Racal 1260-00C.

```
#include <visa.h>
#include <stdio.h>
#include <stdlib.h>

ViSession viRM,m_mod;
int main()
{

unsigned short id_reg,dt_reg ;                /* ID & Device Type Registers */
unsigned short stat_reg, a24_offset ;         /* Status Register & A24 offset
                                                 register */
short value;

ViStatus errStatus;                           /*Status from each VISA call*/

    /* Open the default resource manager  */
errStatus = viOpenDefaultRM ( &viRM);
if (VI_SUCCESS > errStatus){
   printf("ERROR: viOpenDefaultRM() returned 0x%x\n",errStatus);
   return errStatus;}

    /* Open the M-Module instrument session ; Logical Address = 8 */
errStatus = viOpen(viRM,"GPIB-VXI0::8",VI_NULL,VI_NULL,&m_mod);
if (VI_SUCCESS > errStatus){
   printf("ERROR: viOpen() returned 0x%x\n",errStatus);
   return errStatus;}

    /* read  and print the module's ID Register  */
errStatus = viIn16(m_mod,VI_A16_SPACE,0x00,&id_reg);
if (VI_SUCCESS > errStatus){
   printf("ERROR: viIn16() returned 0x%x\n",errStatus);
   return errStatus;}
printf("ID register = 0x%4X\n", id_reg);

    /* read  and print the module's Device Type Register   */
errStatus = viIn16(m_mod,VI_A16_SPACE,0x02,&dt_reg);
if (VI_SUCCESS > errStatus){
   printf("ERROR: viIn16() returned 0x%x\n",errStatus);
   return errStatus;}
printf("Device Type register = 0x%4X\n", dt_reg);
```

```
    /* read and print the module's Status Register  */
errStatus = viIn16(m_mod,VI_A16_SPACE,0x04,&stat_reg);
if (VI_SUCCESS > errStatus){
   printf("ERROR: viIn16() returned 0x%x\n",errStatus);
   return errStatus;}
printf("Status register = 0x%hx\n", stat_reg);

    /* read and print the module's A24 Offset Register  */
errStatus = viIn16(m_mod,VI_A16_SPACE,0x06,&a24_offset);
if (VI_SUCCESS > errStatus){
   printf("ERROR: viOpen() returned 0x%x\n",errStatus);
   return errStatus;}
printf("A24 Offset register value = 0x%hx\n", a24_offset);

    /* Drive Bits 00 and 02 to HI State */
errStatus = viOut16(m_mod,VI_A24_SPACE,0x10,0x05);
if (VI_SUCCESS > errStatus){
   printf("ERROR: viOut16() returned 0x%x\n",errStatus);
   return errStatus;}

    /* Close the M-Module Instrument Session */
errStatus = viClose (m_mod);
if (VI_SUCCESS > errStatus) {
   printf("ERROR: viClose() returned 0x%x\n",errStatus);
   return 0;}

    /* Close the Resource Manager Session */
errStatus = viClose (viRM);
   if (VI_SUCCESS > errStatus) {
   printf("ERROR: viClose() returned 0x%x\n",errStatus);
return 0;}

return VI_SUCCESS;
}
```

Registers in A16 Address Space

Table 2-1 lists the five registers in the A16 memory space. The following paragraphs describe each register.

Table 2-1. VXIbus A16 Memory Instrument Registers

Address Mapping	Registers
00_{16}	VXI ID Register
02_{16}	VXI Device Type Register
04_{16}	VXI Status/Control Register
06_{16}	VXI Offset Register
20_{16}	M-Module Interrupt Control Register

VXI ID Register

The ID Register is a read only register at address 00_h (MSB) and 01_h (LSB).

b+00$_h$	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Undefined															
Read	Device Class		Address Space		Manufacturer ID											

- **Device Class:** this field should always be 11 indicating a register-based device.
- **Address Space:** 00 indicating A16/A24 device
- **Manufacturer ID**: 4091 (decimal) for Racal Instruments.

VXI Device Type Register

The Device Type Register is a read only register at address 02_h (MSB) and 03_h (LSB). Reading this register returns a unique identifier for each M-Module.

b+02$_h$	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Undefined															
Read	Required Memory				M-Module Model Code											

- **Required Memory**: 1111_h indicating 256 byte block required.
- **M-Module Model Code**: $F260_h$ for the Racal M1706.

VXI Status/Control Register

The Status/Control Register is a read/write register (address 04_h and 05_h) that controls the module and indicates its status.

b+04$_h$	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write (Control)	A24 Enable	Reserved													Sysfail Inhibit	Reset
Read (Status)	A24 Active	MODID*	M-Module Device Dependent										Ready	Passed	Device Dependent	

- **A24 Enable.** A 1 in this field means access to the devices A24 registers is enabled.
- **Sysfail Inhibit.** Writing a 1 disables the M-Module from driving the SYSFAIL* line.
- **Reset.** Writing a 1 to this field forces the M-Module to reset.
- **A24 Active.** A 1 in this field indicates the M-Module's registers in A24 memory space can be accessed. Default = 1.
- **MODID*.** A 1 in this field indicates that the M-Module is not selected via the P2 MODID line. A 0 indicates the M-Modules is selected by a high state on the P2 MODID line.
- **Ready.** A 1 in this field indicates that the M-Module is ready to accept commands. A 0 indicates the M-Module is busy and not ready to accept commands.
- **Passed.** A 1 in this field indicates the M-Module passed its self test successfully. A 0 indicates the M-Module is either executing or has failed its self test.

VXI Offset Register

The Offset Register (address 06_h and 07_h) contains the value of the base address for accessing registers in the A24 address space.

b+06$_h$	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	A24 Space Base address for those M-Modules needing A24 memory															
Read	A24 Space Base address for those M-Modules needing A24 memory															

Interrupt Selection Register

The Interrupt Selection Register (base + 20_h) specifies which VXI interrupt line the M-Module will use. M-Modules may generate interrupts to indicate that a command has been completed. These interrupts are sent to and acknowledged by the Slot 0 Module or other system controller via one of seven VXI backplane interrupt lines. Different controllers treat the interrupt lines differently, and you should refer to your controller's documentation to determine how to set the interrupt level. GPIB Command Modules configured as VXI Resource Managers treat all interrupt lines as having equal priority. For interrupters using the same line, priority is determined by which slot they are installed in; lower-numbered slots have higher priority than higher-numbered slots. Slot 0 Modules service line 1 by default, so it is normally correct to leave the interrupt level set to the factory default of IRQ1.

b+20$_h$	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Reserved												INT	VXI Interrupt Line		
Read (default value)	Reserved												INT 1	VXI Interrupt Line 0	0	1

If your controller's documentation instructs you to change the interrupt level, you need to specify the level in the VXI Interrupt Selection Register. To cause the M-Module to interrupt on one of the VXI interrupt lines, write to the appropriate bits (refer to table below). To disable the module's interrupt, set the bits to 000. Selecting other than the default interrupt line 1 is not recommended. Reading the default value of this register returns the value XXX9_h.

Bits 2 - 0	Selected Interrupt Line
000	NONE (Interrupt Disabled)
001	IRQ1 (default)
010	IRQ2
011	IRQ3
100	IRQ4
101	IRQ5
110	IRQ6
111	IRQ7

M-Module specifications define three types of interrupts. The INT bit (bit 3) determines which M-Module interrupt style is supported. If INT is set to a 0, the M-Module supports interrupt types A and B. If INT is set to a 1, the M-Module supports interrupt type C (this is the default).

Type A Interrupts The interrupting M-Module removes the interrupt request upon a register access (software method) to the interrupting M-Module (such as reading the Status Register). DTACK* is not asserted during interrupt acknowledge.

Type B Interrupts The interrupting M-Module removes the interrupt request via a hardware method (on IACK* going low) but provides no vector information for the interrupt. This is the same as Type C interrupts except that no vector is supplied and DTACK* is not asserted.

Type C Interrupts The interrupting M-Module removes the interrupt request via a hardware method and provides an interrupt vector on the data bus and DTACK* is asserted during the interrupt acknowledge cycle. The M-Module removes the interrupt request by IACK* going low.

In VXI specifications however, only two types of interrupts are defined; RORA (Release on Register Access) and ROAK (Release on Acknowledge). The C&H Technologies Model VX405C Carrier converts M-Module Type A interrupts to RORA and Types B and C interrupts to ROAK (default).

RORA Interrupts The interrupting device provides its logical address on the data bus (D0 - D7) during the interrupt acknowledge cycle that was initiated in response to its interrupt request. It does not remove the interrupt request until its Status/Control register is accessed.

ROAK Interrupts The interrupting device removes the interrupt request upon the presence of a properly addressed interrupt acknowledge cycle and provides its logical address on the data bus (D0 - D7). A cause/status byte is also placed on the data bus (D15 - D8)

Registers in A24 Address Space

Table 2-2 shows the register definitions for the Racal M1706.

Table 2-2. Racal M1706 Registers

Word Address (Offset from A24 Base)	Register Name	Register Type
00_h	Status Register	Read Only
02_h	Control Register	Read/Write
04_h - $0E_h$	Reserved	NA
10_h	Output Register	Read/Write
12_h	Output Enable Register	Read/Write
14_h	Input Register	Read Only
16_h	Compare Enable Register	Read/Write
18_h	Compare Data Register	Read/Write
$1A_h$ - $7E_h$	Unused	NA
80_h - FE_h	ID EEPROM	Read/Write

Status Register

This register monitors the module's Ready and Interrupt Status states.

b+00_h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Reserved															
Read	Reserved														Int. Status	Ready

Reset Condition -- Bit 00 = logic "1", Bit 01 = logic "0".

Bit Definitions

Ready -- When set to logic "1", the M-Module is ready to accept read or write instructions. When set to logic "0", the M-Module is busy and will not accept any new instructions.

Interrupt Status -- This bit mirrors the module's interrupt (IRQ) line. When set to logic "1", an interrupt is being asserted. When set to logic "0", interrupt is not being asserted.

Control Register

This register controls module reset (soft reset), interrupt enabling, and debounce enabling.

b+02_h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Reserved													Deb. Cont.	Int. Enable	Reset
Read	Reserved													Deb. Cont.	Int. Enable	Reset

Reset condition -- Bits 00 - 03 = logic "0".

Bit Definitions

Reset -- Writing a logic “1” to this bit initiates a soft reset. Writing a logic “0” to this bit terminates soft reset.

Interrupt Enable -- Writing a logic “1” to this bit enables the M-Module to interrupt upon a pattern match (see "Interrupt Registers" on page 2-15). Writing a logic “0” to this bit disables interrupting.

Debounce Control -- Writing a logic “1” to this bit enables the debounce circuitry. When enabled, input data will incur a 3 ms debounce time period prior to being latched into the Input Register. Writing a logic “0” to this bit disables the debounce circuitry--input data will be immediately latched into the Input Register.

Output Register

This register acts as a latch for data being output from the carrier to the device under test.

b+10$_h$	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Read	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

Reset Condition -- Bits 15 - 00 = logic “0”

Bit Definitions

D00 - D15 -- These are the 16 data output bits corresponding to the data output lines D00 - D15.

Output Enable Register

This register enables/disables output data lines.

b+12$_h$	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Write	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Read	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

Reset Condition -- Bits 15 - 00 = logic “0”

Bit Definitions

D00 - D15 -- These are the 16 output enable bits corresponding to the data output lines D00 - D15. When you write a logic “1” to a specific bit, the corresponding data line is enabled to output data. When you write a logic “0” to a specific bit, the corresponding data line is disabled from outputting data.

Input Register

This register acts as a latch for data being input to the M-Module from the device under test.

b+14$_h$	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Reserved															
Read	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

Reset Condition -- Bits 15 - 00 = logic “0”

Bit Definitions

D00 - D15 -- These are the 16 data input bits corresponding to the data input lines D00 - D15.

Note

If the module is reset, with no loads or signals applied, the input register will contain the value FFFF$_h$ because of the internal pull-up resistors. If you source a low and then perform and then read the input register the response may still show a low. It takes approximately 5µS after the output is disabled for the pull-ups to bring the input circuit up to the minimum 1.8V for a high indication.

Interrupt Registers

An interrupt occurs (if enabled) when an input data pattern matches the pattern stored in the Compare Data Register. You control which data lines will be used in the comparison by enabling/disabling bits in the Compare Enable Register. Additionally, the Interrupt Enable bit in the Control Register must be high for an interrupt to occur.

Compare Enable Register

This register enables/disables bits for interrupt pattern matching.

b+16$_h$	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Read	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

Reset Condition -- Bits 15 - 00 = logic “0”

Bit Definitions

D00 - D15 -- These are the 16 compare enable bits corresponding to the bits in the Compare Data Register. When you write a logic “1” to a specific bit in the Compare Enable Register, that bit will be used in the pattern comparison. When you write a logic “0” to a specific bit, that bit will not be used in the pattern comparison.

Compare Data Register

This register is where you store a data pattern for interrupt pattern matching.

b+18$_h$	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Read	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

Reset Condition -- Bits 15 - 00 = logic "0"

Bit Definitions

D00 - D15 -- These bits contain the pattern to be matched in interrupt pattern comparison.

ID EEPROM Register

The ID EEPROM Register allows you to access the contents of the ID EEPROM. The ID EEPROM contains sixty-four 16-bit words of M-Module ID data and VXI M-Module data.

Note

This register is intended to be used by the higher-level software driver. The software driver must perform a series of many reads and writes to this register to perform the required functions within the EEPROM. **When register programming, it is much easier to read the module ID data from the VXI registers (A16 memory area) instead of reading the ID EEPROM Register.** A16 addressing is discussed earlier in this chapter. Do NOT attempt to read the ID EEPROM. Do not attempt to read the EEPROM Registers.

b+80$_h$ - FE$_h$	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Unused															
Read														Chip Select	Clock	Data In/Out

Reset Condition -- Bits 15 - 08 = logic "1", Bits 07 - Bit 00 = logic "0".

Caution

Do not attempt to write to Bit 00 of the ID EEPROM register. You could possibly write-over the contents of the ID EEPROM.

Bit Definitions

Data In/Out -- Reading this bit returns the value returned from the Data Out pin of the ID EEPROM.

Clock -- Writing a logic "1" to this bit forces the SK pin of the ID EEPROM high and writing a logic "0" drives it low. This bit is used as a clock to the ID EEPROM for reading data out. Reading this bit always returns logic "0".

Chip Select -- Writing a logic "1" to this bit selects the ID EEPROM. Writing a logic "0" to this bit deselects the EEPROM. Reading this bit

always returns logic “0”.

Table 2-3. ID EEPROM Contents

Word Number	Description	ID EEPROM Contents
0	Sync Code	5346_h
1	M-Module Number (binary code)	$069A_h$ (binary-coded 1690)
2	Revision Number (binary code)	0001_h
3	Module Characteristics	0868_h
4 - 7	Reserved	0000_h
8 - 15	Module Dependent	0000_h
16	VXI Sync Code	$ACBA_h$
17	VXI ID	$CFFF_h$
18	VXI Device Type	$F260_h$
19 - 31	Reserved	0000_h
32 - 63	Module Dependent	0000_h

Appendix A
Specifications

M-Module Specification Compliance

The Racal M1706 complies with the Mezzanine M-Module Specification. The Racal M1706 also supports:

- A08, D16 accesses
- INTC interrupts
- IDENT capability

Racal M1706 Specifications

Carrier Interface Specifications

The Racal M1706 incorporates the standard 40-pin, 20x2 row connector interface to the carrier board for power and data/control, but does not have the 24-pin optional connector for carrying user-connections back onto the carrier board.

I/O Lines Specifications

Maximum Output Voltage: +30 VDC (I/O to Chassis or common)

Output Characteristics:
Vout (hi): ≥ 2.9 V @ I_{source} ≤ 20 mA
Vout(lo): ≤ 0.4 V @ I_{sink} ≤ 200 mA

Input Characteristics:
Vin(hi): ≥ 1.8 V
Vin(lo): ≤ 0.8 V

User Connector

44-pin D-Sub connector.

Power Requirements

	I_{PM} (A)	I_{DM} (A)
+5VDC	0.385	0.350
+12VDC	0	0
-12VDC	0	0

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Racal Instruments

REPAIR AND CALIBRATION REQUEST FORM

To allow us to better understand your repair requests, we suggest you use the following outline when calling and include a copy with your instrument to be sent to the Racal Repair Facility.

Model_____ Serial No._____ Date_____

Company Name_____ Purchase Order #_____

Billing Address_____

City

State/Province Zip/Postal Code Country

Shipping Address_____

City

State/Province Zip/Postal Code Country

Technical Contact_____ Phone Number ( ) _____

Purchasing Contact_____ Phone Number ( ) _____

1. Describe, in detail, the problem and symptoms you are having. Please include all set up details, such as input/output levels, frequencies, waveform details, etc.

2. If problem is occurring when unit is in remote, please list the program strings used and the controller type._____

3. Please give any additional information you feel would be beneficial in facilitating a faster repair time (i.e., modifications, etc.)_____

4. Is calibration data required? Yes No (please circle one)

Call before shipping Ship instruments to nearest support office.

Note: We do not accept "collect" shipments.